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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,615	01/30/2004	Paul T. Artman	016295.1560	6751

7590 05/03/2007

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

MAIL DATE	DELIVERY MODE
05/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/768,615	ARTMAN ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10,11,13,14,20,21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10,11,13,14,20,21,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 6-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito, Japanese Application 03-300482, in view of Fairbanks et al., US Patent 5307003, hereinafter Fairbanks.

3. In re claim 1, Saito discloses a method for managing power consumption in a computer system having a processor [constitution in reference to conventional setup with total rated capacity set to 150 A], comprising the steps of:

- Providing an array of redundant power supplies [8a-8c], wherein each power supply in the array is rated to a power delivery capacity [e.g., 50 A] that is less than the maximum power draw [e.g., 150 A] of the computer system [0012-13].
- Identifying the loss of operation of a power supply of the redundant power supply array, wherein the total rated capacity of the functioning power supplies [e.g., 100 A] of the array is less than the total rated capacity of the fully operational array [e.g., 150 A] [0012; conventional setup with total rated capacity set to 150 A].

4. Saito did not disclose explicitly the details of the computer system operation.

5. Fairbanks discloses a method comprising identifying the status of a power supply [battery] and reducing the operating speed [frequency] of the processor of the computer system [col.3, ll.12-20].

6. It would have been obvious to one of ordinary skill in the art, having the teachings of Saito and Fairbanks before him at the time the invention was made, to modify the system taught by Saito to include the teachings of Fairbanks, in order to obtain the claimed method [inoperable battery voltage condition analogous to loss of power supply]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to preserve the integrity of data [Fairbanks: col.3, ll.12-20; preserving the integrity of data is even more pertinent to conventional setup disclosed by Saito where the total rated capacity of the functioning power supplies under a loss may not be conducive to continual operation].

7. As to claim 2, Fairbanks discloses, wherein the step of reducing the operating speed of the processor of the computer system comprises the step of asserting a signal to an input of the processor to cause the processor enter a power management mode [mode associated with word processing] [col.2, ll.10-16; col.8, ll.20-29].

8. As to claim 6, Fairbanks discloses, comprising the step of increasing the operating speed of the processor in conjunction with the operation of all power supplies [of the redundant power supply array] [col.8, ll.35-39; operation of all power supplies of the redundant power supply array allows computer system to increase power draw up to maximum – increase power draw increases operating speed].

9. In re claim 7, Saito discloses a computer system [0001 industrial application], comprising:

- An array of redundant power supplies [8a-8c], wherein each power supply of the array is rated to a power delivery capacity [e.g., 40A, 50 A, 60A] that is less than the maximum power draw [e.g., 150 A] of the computer system [0012-13].
- A processor [0001 industrial application].
- Identifying the loss of a power supply of the array of redundant power supply [0012] whereby the power draw of the computer system is reduced to a level below [e.g., 100A] the rated capacity [e.g., 120A] of the functioning power supplies of the array [0013; 40A goes down and replaced by 60A – rated capacity becomes 120A], and wherein the rated capacity of the functioning power supplies of the array is less than the total rated capacity of the fully operational array [0012; conventional setup with total rated capacity set to 150 A].

10. Saito did not disclose explicitly the details of the computer system operation.

11. Fairbanks discloses a computer system comprising a processor wherein the operating speed [frequency] of the processor is reduced upon a status of a power supply [battery] [col.3, ll.12-20].

12. It would have been obvious to one of ordinary skill in the art, having the teachings of Saito and Fairbanks before him at the time the invention was made, to modify the system taught by Saito to include the teachings of Fairbanks, in order to obtain the claimed system [inoperable battery voltage condition analogous to loss of power supply]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to preserve the integrity of data [Fairbanks: col.3, ll.12-20].

13. As to claim 8, Saito and Fairbanks discloses each and every limitation as discussed above in reference to claim 2.

14. As to claim 10, Saito discloses, wherein the array of redundant power supplies includes an array controller [supervisory circuit] for identifying the failure or removal of a power supply of the array [0015].

15. Claims 4-5, 11, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito and Fairbanks as applied to claims 1, 7 above, and further in view of Chen et al., US Publication 20040255174, hereinafter Chen.

16. Saito and Fairbanks taught each and every limitation of the claim, as discussed above. Saito and Fairbanks did not disclose the details of identifying the loss of operation of a power supply.

17. In re claim 4, Chen discloses a method for managing power consumption in a computer system, comprising the step of identifying the loss of operation of a power supply that comprises the step of notifying the BIOS [22] of the computer system of the loss of operation of a power supply [0022].

18. It would have been obvious to one of ordinary skill in the art, having the teachings of Chen, Saito and Fairbanks before him at the time the invention was made, to modify the system taught by Saito and Fairbanks to include the teachings of Chen, as BIOS are well known soft/firmware components adaptable to handle a wide variety of input/output signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to smooth power transitions [Chen: 0022].

19. As to claim 5, Chen discloses, wherein the signal [e.g., to lower frequency] at the processor [20] is asserted by the BIOS of the computer system.[fig.2, 0022; power supply signal inputted to BIOS to induce the appropriate operating frequency].

20. As to claim 11, Chen discloses each and every limitation as discussed above in reference to claims 4 and 5.

21. As to claim 14, Chen discloses, comprising a BIOS for receiving an indication of a loss of a power supply and for asserting a signal to reduce the data rate of the front side bus [26] of the processor [0022; lowering the frequency lowers the data rate].

22. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Saito and Fairbanks as applied to claim 11 above, and further in view of Wittlinger, US Publication 20040178940.

23. Chen, Saito and Fairbanks taught each and every limitation of the claim, as discussed above. Chen, Saito and Fairbanks did not disclose explicitly lowering a lower voltage level to be applied to the processor.

24. Wittlinger discloses a method comprising asserting a signal to cause a lower voltage level to be applied to the processor [0002].

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Chen, Wittlinger, Saito and Fairbanks before him at the time the invention was made, to modify the system taught by Chen, Saito and Fairbanks to include the teachings of Wittlinger, in order to obtain the claimed system [i.e., lowering the frequency and voltage reduces power consumption]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [Wittlinger: 0002].

26. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of Levin et al., US Patent 5841313, hereinafter Levin.

27. In re claim 20, Saito discloses a method for reducing the power draw of a computer system having an array of redundant power supplies [8a-8c], wherein each power supply in the array is rated to a power delivery capacity [e.g., 50 A] that is less than the maximum power draw [e.g., 150 A] of the computer system [0012-13], comprising the step of identifying the loss of operation of a power supply of the redundant power supply array, wherein the total rated capacity of the functioning power supplies of the array is less than the total rated capacity of the fully operational array [0012; conventional setup with total rated capacity set to 150 A].

28. Saito did not disclose explicitly the details of the computer system operation.

29. Levin discloses a method for reducing the power draw of a computer system [col.3, ll.36-67], comprising the steps of:

- Determining whether the power draw of the computer system has reached or exceeds a predetermined threshold level [col.4, ll.2-17].
- Causing a processor to enter a power conservation state [sleep] when the power draw of the computer system reaches or exceeds the threshold level [col.4, ll.2-17; switches to sleep upon reaching threshold].

30. It would have been obvious to one of ordinary skill in the art, having the teachings of Saito and Levin before him at the time the invention was made, to modify the system taught by Saito to include the teachings of Levin, as the use of power conservation state such as sleep state is very well known in the art for reducing power consumption and suitable for use in the system

of Saito. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power leakage [Levin: col.3, ll.36-67].

31. As to claim 21, Levin did not disclose explicitly that entering the sleep [power conservation] state comprises reducing the effective rate of at least one internal clock of the processor by turning on and off according to a duty cycle. Examiner had taken Official Notice that it is well known in the art to reduce the effective rate of at least one internal clock of the processor when entering the sleep state; and it is well known in the art to reduce the operating speed of the processor by throttling a processor – i.e., asserting a signal to an input of the processor to cause the processor to turn a clock of the processor on an off according to a duty cycle. It would have been obvious to one of ordinary skill in the art, having the teachings of Saito and Levin before him at the time the invention was made, to explicitly include the reduction of the effective rate of at least one internal clock by throttling the processor in order to obtain a sleep state. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to reduce power consumption when entering a sleep state.

32. Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito and Levin as applied to claim 20 above, and further in view of Wittlinger, as applied to claim 13 above.

33. Claims 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito and Levin as applied to claim 20 above, and further in view of Chen, as applied to claim 14 above.

Response to Arguments

Applicant's arguments filed April 6, 2007 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
April 26, 2007

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/30/07